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High-Speed Vertical InGaAs Nanowire Transistor Technology for RF BEOL Integration

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Summary

We have developed a new RF-compatible process for vertical InGaAs nanowire MOSFETs on silicon substrates. We have improved scalability by replacing the previously used interlayer openings to gate and source with metal plugs. The top interlayer that was previously a hardbaked photoresist is now a standard low-k dielectric layer that is used in our front-side BEOL technology. The presented devices show good performance but need further scaling to reach state-of-the-art metrics. Integrated, the high-speed vertical transistors and low-loss BEOL available at Lund University can form a test vehicle for terahertz circuit design.

1. Introduction

An analog performance gap towards terahertz frequencies (0.1-1 THz) motivates the use of III-V semiconductor materials. Low noise, high-speed semiconductor THz circuit technologies utilize InGaAs channel high electron mobility transistors (HEMTs) [1], and record transconductance is provided by lateral InGaAs channel metal-oxide-semiconductor field effect transistors (MOSFETs) [2]. However, modulation doped HEMTs are optimized for speed but provide limited engineering possibilities for improved voltage handling. The vertical InAs/InGaAs heterostructure nanowire MOSFET, by contrast, allows bandgap engineering for breakdown voltage management [3]. Vertical nanowire channels also demonstrate high transconductance and low leakage current due to strong electrostatic control in the gate-all-around geometry [4].

Vertical nanowire MOSFETs need multiple channels for current drive and analog performance. One challenge is controlled formation of a radio frequency (RF) compatible low-capacitance low-resistance interface to the nanowires. The front-end-of-line (FEOL) core device must also be compatible with the back-end-of-line (BEOL) process technology. A low-loss front-side BEOL based on microstrip lines in gold metallization and benzocyclobutene (BCB) interlayer dielectrics is available [5]. In this work, a new FEOL process scheme was developed to address these issues. We present DC and RF characteristics of a MOSFET using the refined process. It achieves a maximum oscillation frequency, f_{max}, of 53 GHz at a relaxed gate-length and a coarse interface routing design. Layout optimization and BEOL integration will be future topics of interest.

2. Device Fabrication

A schematic cross section of the vertical nanowire MOSFET device structure is shown in Fig. 1(a). We have revised the previous fabrication process [4] to enable minimalistic finger patterning without use of access pads, avoiding finger release etching. Connections to gate and source instead use highly scaled metal plugs. Mid-process electron micrographs of a gate finger with wires and fingers with plug connectors are shown in Fig. 1(b-c), respectively. Each gate plug connects a gate finger and an array of source plugs are connecting the InAs mesa source contact consisting of a 60 nm thick layer of W. Fabrication of the plugs were performed using e-beam evaporation of Ti/Au, with a thickness of 5/500 nm, and a lift-off process. Due to the need for precise alignment and the small size of the structures, the pattern was created using electron beam lithography (EBL) and with a bilayer consisting of LOR10A and PMMA 950 A6. Additionally, in this process the top spacer was switched to BCB by spinning Cyclotene 3022-35 and hard curing it, followed by a RIE back etch to set the spacer thickness. An optical micrograph of the finalized device is shown in Fig. 1(d), with various features visible through the interlayers.

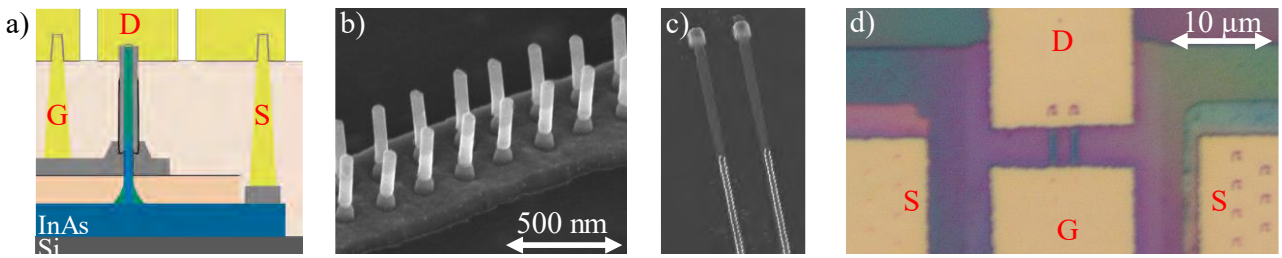

Figure 1. Schematic cross section image of the nanowire MOSFET is shown in (a). Mid-process SEM images of nanowires protruding from the gate metal and an overview of two 400 nm wide fingers with gate plugs are shown in (b) and (c), respectively. An optical top view of the completed device is shown in (d).

3. Device Characterization

A device consisting of 80 nanowires divided over two gate fingers (2x40) is presented. The channel diameter is 25 nm and the gate length is 110 nm. Transfer and output characteristics are shown in Fig. 2(a-b), respectively. Even though it is a long channel device, it shows normalized g_m of 0.5 mS/µm and R_{on} of 1140 Ωµm at V_d = 0.5 V. The minimum subthreshold swing is 96 mV/dec. High frequency characteristics were measured with an Agilent E8361A PNA, 10 MHz-67 GHz. The measured gain parameters at biasing V_{gs} = 0.25 V and V_{ds} = 0.7 V are shown in Fig. 2(c). The device has a current gain transition frequency, f_T, of 17 GHz and an f_{max} of 53 GHz. Also shown, in good agreement with measurement, is the response of a simple small signal model (hybrid pi with static parasitic shells). The cold FET method was used to identify extrinsic model parameters [6].

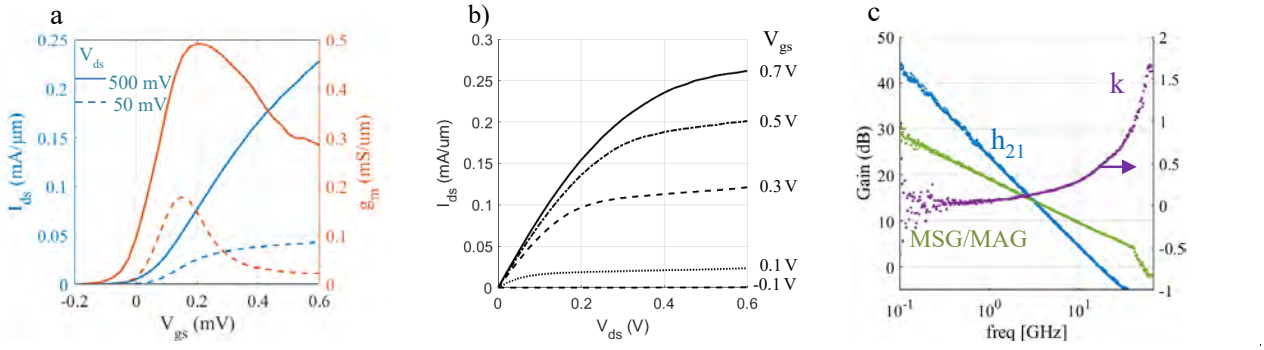

Figure 2. DC measurements of transfer (a) and output (b) characteristics of the nanowire MOSFET. Measured and modeled gain for V_{gs} at 0.25 V and V_{ds} of 0.7 V is shown in (c). This resulted in f_T and f_{max} at 17 GHz and 53 GHz respectively.

Intended as a test vehicle for process revision, a safe gate length and conservative design of electrode layers was used in this work. This means that, *e.g.*, layout and vertical scaling has significant margins. The achieved gain transition values are thereby encouraging. Strong performance improvements should be expected if sizing and process control is correctly managed.

4. Conclusion

We present a new RF compatible process for the fabrication of vertical InAs/InGaAs nanowire MOSFETs. This process has addressed known bottlenecks and utilizes metal plug terminal contacts and a BCB interlayer dielectric. This provides a critical step towards unprecedented compatibility with established RF BEOL technology. We have, through this achievement, moved the process towards a higher technology readiness level. Future work includes scaling of the device layout and nanowire geometry, plus BEOL verification, towards a technology platform with high speed MOSFETs for terahertz circuit demonstrations.

5. Acknowledgements

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References

[1] H. B. Jo *et al.*, “L g = 25 nm InGaAs/InAlAs high-electron mobility transistors with both f T and f max in excess of 700 GHz,” *Appl. Phys. Express*, vol. 12, no. 5, 2019, doi: 10.7567/1882-0786/ab1943.

[2] J. Lin, X. Cai, Y. Wu, D. A. Antoniadis, and J. A. Del Alamo, “Record Maximum Transconductance of 3.45 mS/µm for III-V FETs,” *IEEE ELECTRON DEVICE Lett.*, vol. 37, no. 4, 2016, doi: 10.1109/LED.2016.2529653.

[3] O. Kilpi, S. Andri, J. Svensson, S. R. Mamidala, E. Lind, and L. Wernersson, “Increased Breakdown Voltage in Vertical Heterostructure III-V Nanowire MOSFETs with a Field-Plate,” pp. 7–10.

[4] O. P. Kilpi *et al.*, “High-Performance Vertical III-V Nanowire MOSFETs on Si with gm> 3 mS/µm,” *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1161–1164, 2020, doi: 10.1109/LED.2020.3004716.

[5] S. Andric, L. Ohlsson Fhager, F. Lindelöw, O.-P. Kilpi, and L.-E. Wernersson, “Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs,” *J. Vac. Sci. Technol. B*, vol. 37, no. 6, p. 061204, Nov. 2019, doi: 10.1116/1.5121017.

[6] Y. L. Lai and K. H. Hsu, “A new pinched-off cold-FET method to determine parasitic capacitances of FET equivalent circuits,” *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 8, pp. 1410–1418, 2001, doi: 10.1109/22.939921.